

71 100

FIG. 2

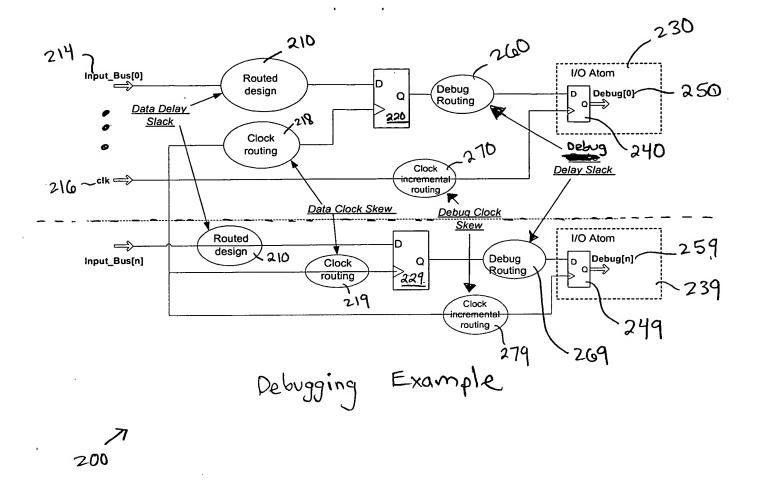
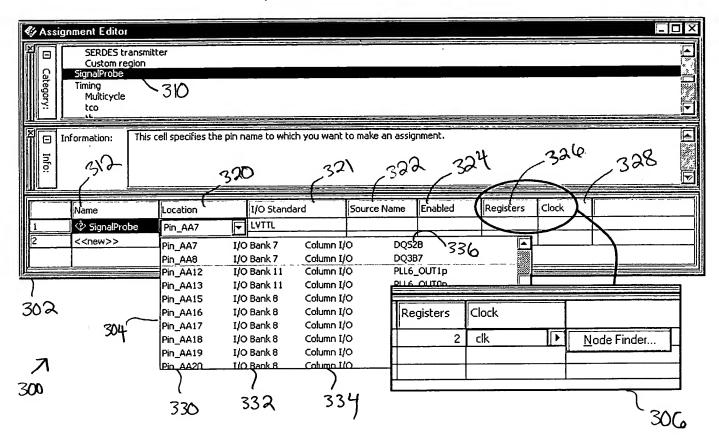
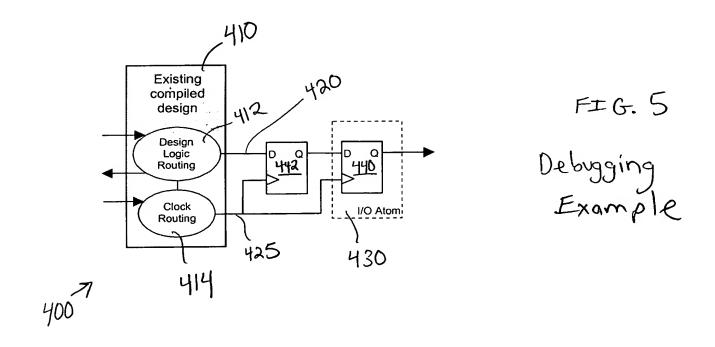


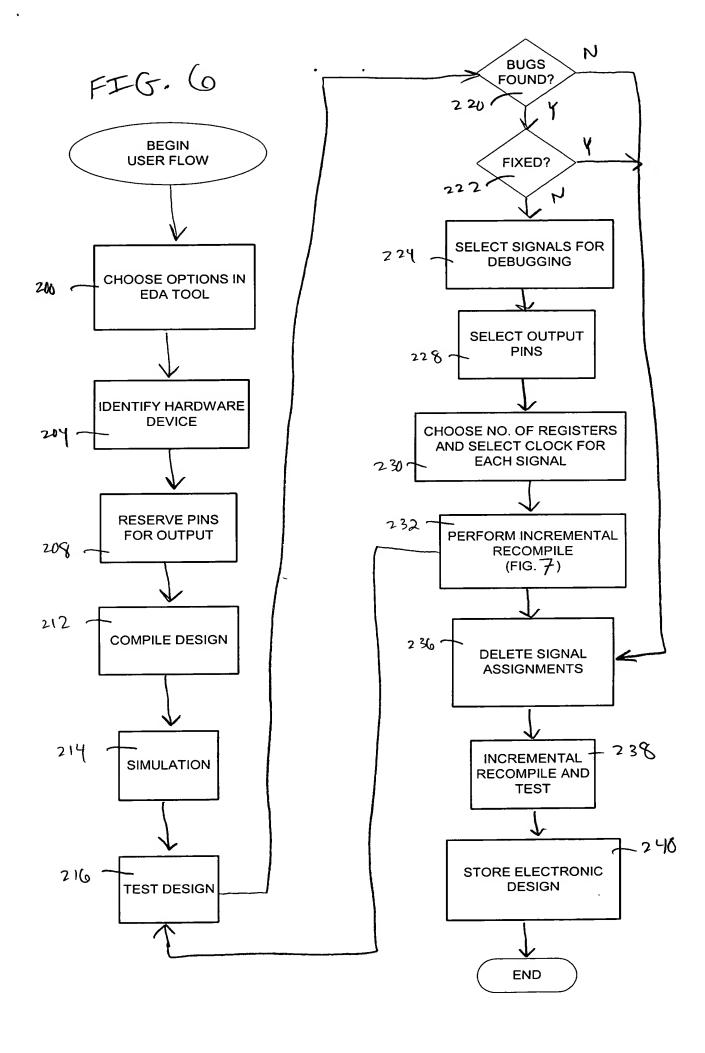
FIG. 3

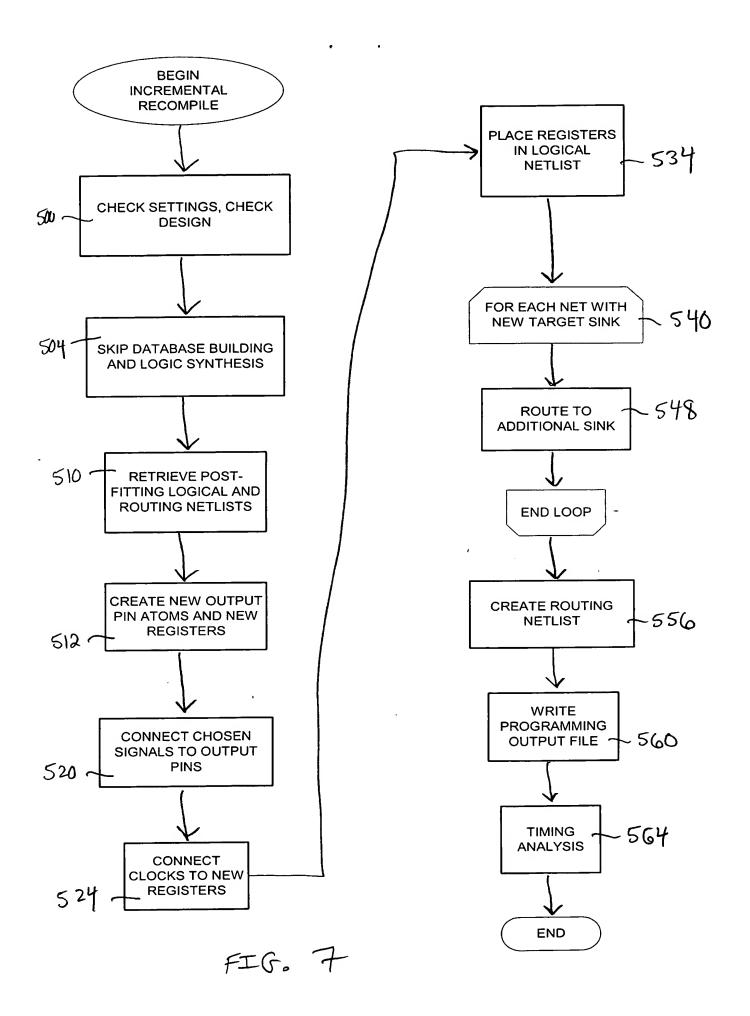
## BEST AVAILABLE COPY

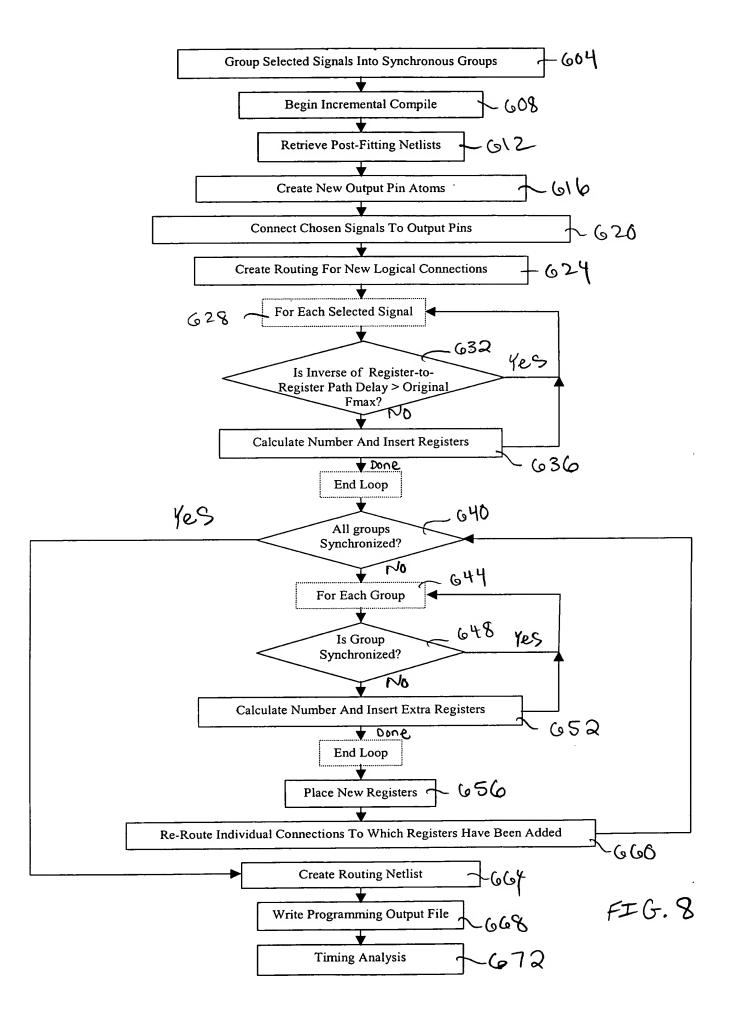
FIG. 4 User Interface Example











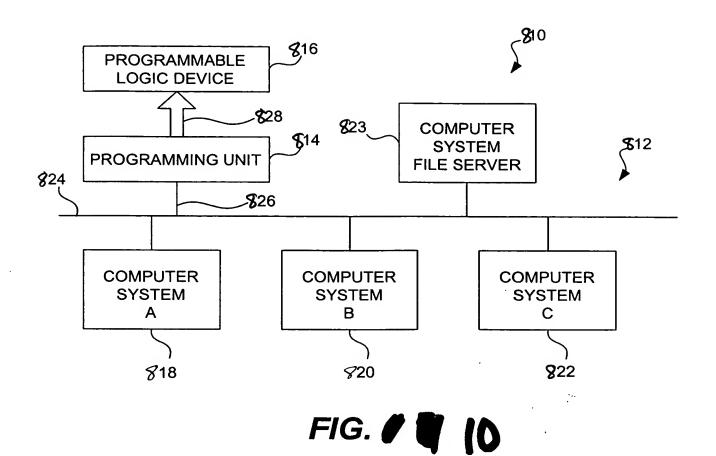
## BEST AVAILABLE COPY

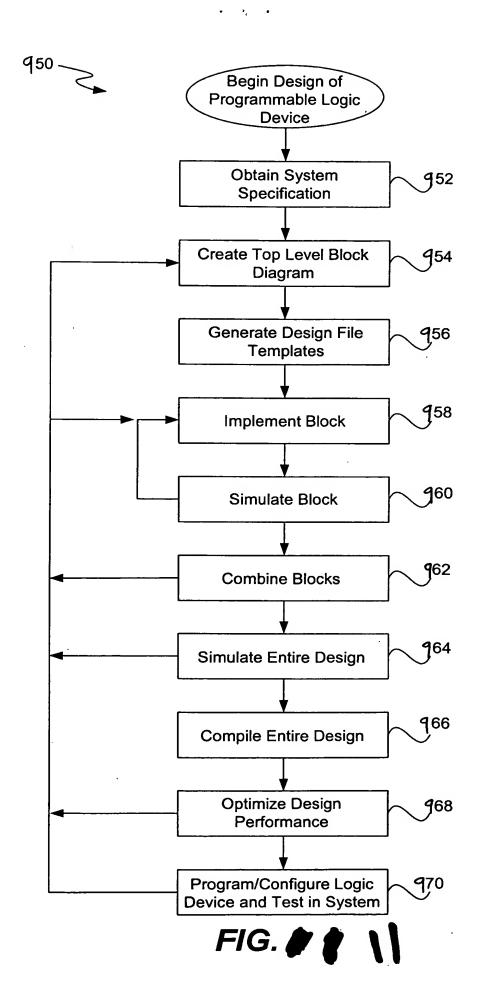
FIG. 9 Timing Report Table

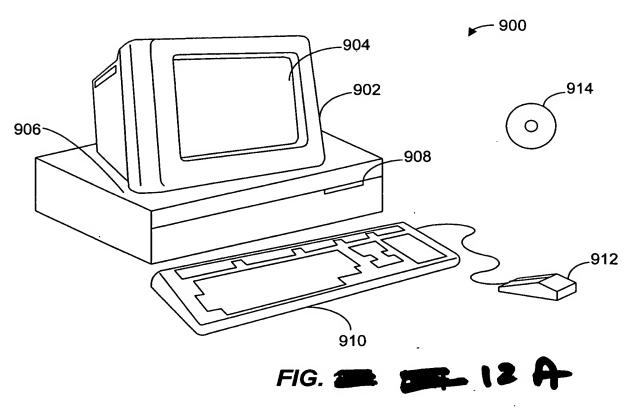
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hus aken Compilation Report	and the second s					
Compilation Report		अक्ष प्रताम (प्रतिकार), त्रिक्साम्बर्धेक				
■ Legal Notice	Source Nam	e: (Fin Location	Pin Name	Enable	Status:	Delay (ns).
Flow Summary	it reg2	Pin_H35	sp2	On .	Routed	8.786 ns
Flow Settings	2 reg1	Pin_U26	sp1	On	Routed	8.747 ns
Flow Elapsed Time 750 —	12-2	Pin_P27	sp_test	On	Routed	5.808 ns
■ Flow Log	3 pin_o0 4 reg0	Pin_F35	sp0.	0n	Routed	Registered
Analysis & Synthesis	5 reg3.	Pin_H34	sp3	On	Routed	Registered
Fitter Sim Assembler 708	₿ .reģ4	Pin_U27	sp4	On	Routed	Registered
Assembler 10 8	7 reg5	Pin_T27	sp5	On		Registered
Timing Analyzer Settings	8 reg6	Pin_G35	sp6·	On	Routed	Registered
Timing Analyzer Summary	(§ reg7	Pin_G34	sp7	On	Routed	Registered
Clock Settings Summary	100	1: :::_ 3	Top.	13.1	7	)
Clock Setup: 'clk'			(	l		7~~
	730	732	734	736	738	739
Set too	/30		,	, , ,	,	i.
tpd						į.
- Source to Output Deley's						i
-: Esth						
Se Minimum too 7/2		7.1				1
Minimum tpd	716					
Timing Analyzer Messages						ı
-	: 1 <b>조건</b>					1.4







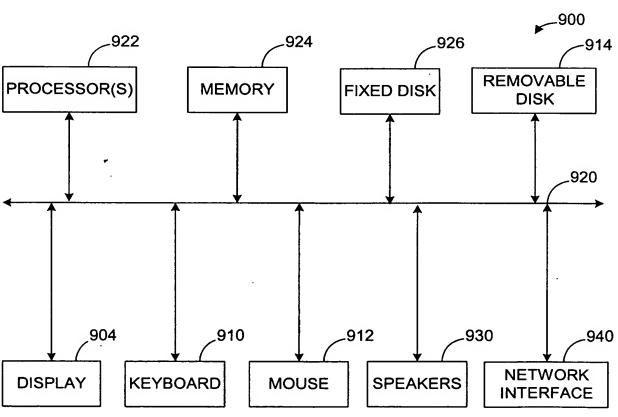


FIG. - 12B